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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,440	11/14/2003	Damien Lenoble	02GR126654484	9369

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ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER	
LUU, CHUONG A	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,440	LENOBLE, DAMIEN	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-46 and 54-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-46 and 54-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 25-41, 43-46 and 54-62 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECITONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 25-41, 43-46 and 54-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chidambaram et al. (U.S. 6,682,980 B2) in view of Yu (U.S. 6,235,599 B1).

Chidambaram discloses a PMOS transistor with

(25); (54) forming a gate (104) on a silicon substrate(106) (see Figure 5);

implanting dopants in the amorphous silicon regions to form drain and source extensions therein (see Figure 6);

amorphizing regions the silicon substrate to obtain amorphous silicon regions adjacent the gate after implanting the dopants (see Figure 7);

forming drain and source regions in the respective drain and source extensions with a channel being defined therebetween, the drain and source regions being formed at a temperature (see Figures 5-7);

(26); (56) wherein the silicon substrate comprises a crystalline silicon substrate (see Figure 5);

(27) further comprising forming spacers on the silicon substrate adjacent the gate after forming the drain and source extensions (see Figures 5-7);

(29) wherein implanting the dopants to form the drain and source extensions comprises performing a deep amorphization the silicon substrate (see Figure 6);

(30) further comprising recrystallizing the silicon substrate after performing the deep amorphorization (see Figures 5-10);

(31) wherein forming the drain and source regions comprises implanting dopants therein (see Figures 5-10);

(32) further comprising recrystallizing the silicon substrate after forming the drain and source regions (see Figures 5-10);

(34) further comprising annealing the silicon substrate after forming the spacers (see Figure 6);

(35) further comprising forming pockets in the silicon substrate, the pockets being doped with a dopant having an opposite conductivity to the dopant implanted when forming the drain and source regions (see Figures 5-10);

(36) wherein the pockets are formed before the amorphized regions are formed; (see Figures 5-10)

(37) wherein the pockets are formed after the amorphized regions are formed (see Figures 5-10);

(38) wherein the pockets are formed before the amorphized regions are formed, and before the dopants are implanted in the silicon substrate (s see Figures 5-10);

(39) wherein the spacers are formed after forming the drain and source extensions (see Figures 5-10);

(40) wherein the spacers are formed before the amorphized regions are formed (s see Figures 5-10);

(44); (62) wherein amorphizing the regions of the silicon substrate comprises implanting ions therein (see Figures 5-10);

(57) further comprising forming spacers on the silicon substrate adjacent the gate after forming the drain and source extensions;

annealing the silicon substrate after forming the spacers (see Figures 5-10);

(58) wherein implanting the dopants form the drain and source extensions comprises performing a deep amorphization in the silicon substrate; further comprising recrystallizing the silicon substrate after performing the deep amorphorization (see Figures 5-10);

(59) wherein forming the drain and source regions comprises implanting dopants therein; and further comprising recrystallizing the silicon substrate after forming the drain and source regions (see Figures 5-10);

(60) further comprising forming pockets in the silicon substrate, the pockets being doped with a dopant having an opposite conductivity to the dopant implanted when forming the drain and source regions (see Figures 5-10).

Chidambaram teaches the above outlined features except for the drain and source regions being formed at a temperature below 800°C; the amorphized regions have a thickness that is greater than 100 nanometers. However, Yu. discloses an integrated circuit with **(25); (54).....** the drain and source regions being formed at a temperature below 800°C (see column 7, lines 29-40. Figure 6); **(28)** further comprising annealing the silicon substrate at a temperature below 800C after forming the drain and source extensions (see c column 7, lines 29-40); **(33)** wherein forming the spacers comprises annealing the silicon substrate at a temperature below 800C (see column 7, lines 29-40); **(43)** wherein the source and drain regions are formed by annealing the silicon substrate at a temperature below 800C (see column 7, lines 29-40. Figures 6-8); **(45)** wherein the ions comprise least one of silicon, germanium, argon, neon, zenon and krypton (see column 5, lines 47-50); **(46)** wherein the dopants being implanted to form the drain and source extensions comprise at least one of B+, BF2+, As+,P+ and Sb+ (see column 5, lines 47-55. Figures 6-8); **(55)** wherein the temperature within a range 800C (see column 7, lines 29-40). Also, Chidambaram and Yu do not explicitly disclose the amorphized regions have a thickness that is greater than 100 nanometers. However, the amorphized regions have a thickness that is greater than 100 nanometers is considered to be obvious. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the

amorphized regions have a thickness that is greater than 100 nanometers Chidambaram 's devices (in accordance with the teaching of Yu) within the range as claimed for the purpose of obtaining the better performance, and it also has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP 2144.05). Also, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
March 17, 2005